UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/984,563	12/03/1997	JEFFREY S. MAILLOUX	95-0653.03	2304

7590 08/30/2006

SCHWEGMAN LINDBERG
WOESSNER & KLUTH, PA
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
KIM, HONG CHONG	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/984,563	MAILLOUX ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-39,59-69 and 75-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-39,63,64 and 75-83* is/are allowed.

6)☒ Claim(s) *59-62 and 65-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 36-39, 59-69 and 75-83 are presented for examination. This office action is in response to the amendment filed on 7/10/06.

Specification

2. Applicants are requested to update the status of the related U.S. patent application referred on page 1 in the application filed and the status of the related U.S. patent applications, accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.). Also applicants are requested to include the status of the related U.S. applications or patents in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 7/10/06 is being considered by the examiner.

DOUBLE-PATENTING

4. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public

policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 65-67 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1,4, 7, 11, 12, and 15 of Mailloux et al.,(Mailloux) US Patent No. 6,615,325 in view of Ogawa U.S. Patent 5,293,347.

As to claims 65, Mailloux discloses receiving a mode select signal (claim 15, maintaining a mode select signal to select a burst mode of operation); receiving an initial external address (claim 15 receiving an initial external address); cycling a second

enabling signal multiply between inactive and active (claim 15 cycling a second enabling signal multiply between inactive and active); generating an internal address on a cycle of the second enabling signal based on the initial external address (claim 15 generating an internal address on a cycle of the second enabling signal based on the initial external address); changing the mode select signal to select a pipeline mode of operation while maintaining the first enabling signal in the active state (claim 15 changing the mode select signal to switch the mode of operation to a pipeline mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state); and receiving an external address on each cycle of the second enabling signal (claim 15 receiving an external address on each cycle of the second enabling signal). However, Mailloux fails to disclose the step of selecting a read or a write operation of the memory.

It would have been readily appreciated by one of ordinary skill in the memory art that a method for accessing a memory comprising a step of selecting a read or a write operation so that it can load or store data from or to a memory unit. *Ogawa* discloses the step of selecting a read or a write operation of the memory (Fig. 1 Ref /WE) for the purpose of controlling a memory access operation thereby preventing an access error.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of selecting a read or a write operation of the memory as taught by Ogawa in the system of Mailloux for the advantages stated above.

As to claims 66, Mailloux further discloses maintaining a first enabling signal in an active state (claim 7 maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal); maintaining a mode select signal to select a burst mode of operation (claim 7 maintaining a mode select signal to select a burst mode of operation; receiving an initial external address (claim 7 receiving an initial external address); cycling a second enabling signal multiply between inactive and active (claim 7 cycling a second enabling signal multiply between inactive and active); generating an internal address on a cycle of the second enabling signal based on the initial external address (claim 7 generating an internal address on a cycle of the second enabling signal based on the initial external address); and switching the mode select signal to select a pipeline mode of operation while maintaining the first enabling signal in an active state (claim 7 changing the mode select signal to select a pipeline mode of operation while maintaining the first enabling signal in an active state). *Ogawa* further disclose the step of selecting a read or a write operation of the memory (Fig. 1 Ref. /WE).

As to claims 67, Mailloux further discloses maintaining a first enabling signal in an active state (claim 4, maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal); maintaining a mode select signal to select a burst mode of operation (claim 4 maintaining a mode select signal to select a first mode); receiving a stream of addresses and cycling a

second enabling signal for processing the stream of addresses (claim 4 receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses); and changing the mode select signal to select a pipeline mode of operation (claim 4 changing the mode select signal to select a second mode while maintaining the first enabling signal in the active state).

Ogawa further disclose the step of selecting a read or a write operation of the memory (Fig. 1 Ref. /WE).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 59-62, 68, and 69 are rejected under 35 U.S.C. 103(a) as obvious over by *Manning*, U.S. Patent 5,610,864 in view of Roy U.S. Patent No. 6,065,092 or *Ogawa* U.S. Patent 5,293,347.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); choosing whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 40-55) or a page mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write

circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 60, *Manning* further discloses a burst mode (col. 6 lines 14-26 & col. 7 lines 43-54 and Fig. 1). *Roy* further discloses the pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62). *Ogawa* further discloses the pipeline mode (abstract and col. 4 lines 9-12, 57-61,& col. 22+).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE). *Ogawa* further discloses switching between a read and a write operations (Fig. 1 /WE).

As to claim 62, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+, switching between reads on this limitation).

As to claim 68, *Manning* discloses a method for data transfer direction selection in a memory (Fig. 1), comprising: selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); selecting a burst (col. 6 lines 14-26 and col. 7 lines 40-55) or a page mode of operation (col. 6 lines 14-21 and col. 7 lines 40-55) for the memory and selecting an external address only path, obtaining external address when the page mode operation is selected (by definition of a page mode, since a new external column address is provided every CAS cycle in the page mode, col. 1 lines 32-36); and selecting an initial buffered external address data path, obtaining an initial external column address, accessing the memory, and generating internal column address when the burst mode operation is selected (by definition of a burst mode, col. 5 lines 50-57). Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the

memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 69, *Manning* discloses a storage device (Fig. 1), comprising: mode circuitry configured select between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a page mode of operation (col. 6 lines 14-26 and col. 7 lines 40-55); selection circuitry for selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); an external column address data path for page read and write operation column address retrieval (by definition of a

page mode, since a new external column address is provided every CAS cycle in the page mode, col. 1 lines 32-36), an internal column address generation module for burst read and write operation column address generation (by definition of a burst mode, col. 5 lines 50-57); and page/burst circuitry coupled to the mode selection circuitry and configured to switch between page mode and the burst mode for operating the storage device in either mode (col. 6 lines 14-26 and col. 7 lines 40-55).

Although Manning discloses "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of

increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Roy discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one

of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by

providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Response to Arguments

7. Applicant's arguments filed on 7/10/06 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Manning discloses a method of accessing a memory (Fig. 1) including "Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS" (col. 5 lines 43-49 in Manning) and "switching between fast page mode, EDO page mode, static column mode and burst operation (col. 7 lines 40-55), in other words, the

pipelined architecture can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed.

However, Manning does not specifically disclose detailed operation of a pipeline mode. It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously and also It was well known in the memory art to include the memory selectively operable in a pipeline mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area. *Roy* discloses the memory selectively operable in a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Alternatively, Ogawa discloses the memory selectively operable in a pipeline mode (abstract, col. 4 lines 9-12, 57-61,& col. 3 lines 22+ and Figs. 7& 8) for the purpose of resulting in high speed read/write operation (col. 3 lines 46-51).

One of ordinary skill in the memory art familiar with Manning, and looking at Ogawa would have recognized that the memory access performance of Manning would have been enhanced by including a pipeline mode in the memory because it would

provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the page mode of Manning to a pipeline mode of Ogawa because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., column-based switching and row-based switching) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore broadly written claims are disclosed by the references cited.

Allowable Subject Matter

8. It appears that claims 36-39, 63-64, and 75-83 are contained allowable subject matter. Claims 65-67 would be allowable if overcame double patenting rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
August 28, 2006